Docket: 14467.05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	John P. Snyder		
Application No.:	10/796,514		
Filing Date:	March 9, 2004	Examiner:	Not Yet Known
Title:	TRANSISTOR HAVING HIGH DIELECTRIC CONSTANT GATE INSULATING LAYER AND SOURCE AND DRAIN FORMING SCHOTTKY CONTACT WITH SUBSTRATE	Group Art Unit:	2811

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this document is being sent via First Class U.S. mail addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on this 19th day of November, 2004.

Susan Nienaber

Susan Nienaber

Dear Sir:

Pursuant to 37 CFR § 1.97(b), the references listed on the attached Form PTO-1449 (1 sheet, submitted in duplicate) are brought to the attention of the Examiner for consideration in connection with the examination of the above-identified patent application. This IDS is being filed before the mailing of a first office action on the merits. In accordance with 37 CFR § 1.97(b), no statement or fee is required.

Copies of the references cited are not enclosed, as allowed under 37 CFR § 1.98(d). Each item on the enclosed Form PTO-1449 was cited to, or cited by, the Office in one or more of the following prior related cases, to which priority to an earlier effective filing date is claimed under 35 U.S.C. § 120, in the present application.

10/215,447 filed August 9, 2002

09/928,124 filed August 10, 2001

09/928,163 filed August 10, 2001

09/777,536 filed February 6, 2001 now U.S. Pat. No. 6,495,882 Issued December 17, 2002

Respectfully submitted,

DORSEY & WHITNEY LLP
Customer Number 25763

Date: November 19, 2004

By: _____

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PTO/SB/08A (10/01) (modified)
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Sheet 1 of 7	**Attorney Docket Number**	**14467.05**

U.S. PATENT DOCUMENTS

*Examiner Initials	Cite No.	DOCUMENT NUMBER Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 4,053,924	10-11-1977	Roman et al.	
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		US- 4,485,550	12-4-1984	Koeneke et al.	
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		EP	0 603 102 A2	6-22-1994			☒	☐
		WO	01 45157	06-21-2001	Spinnaker Semiconductor, Inc.		☐	☐
		JP	06097109	04-08-1994	Fujitsu Ltd		☐	☐
		JP	2000124329	04-28-2000	Toshiba Corp.		☐	☐
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		US- 5,883,010	3-16-1999	Merrill et al.	
		US- 6,037,605	3-14-2000	Yoshimura	
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		US- 6,420,742	7-16-2002	Ahn et al.	
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		US- 6,509,609	1-21-2003	Zhang et al.	
		US- 6,555,879	4-29-2003	Krivokapic et al.	
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		US- 5,040,034	8-13-1991	Yoshinori et al.	
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OTHER DOCUMENTS - NON-PATENT LITERATURE DOCUMENTS

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		LEPSELTER, M.P., SZE, S.M. SB-IGFET: An Insulated Gate Field Effect Transistor Using Schottky Barrier Contacts for Source and Drain. Proceedings of the IEEE, August 1968; pp. 1400-1402.	☐	☐
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		KOENEKE, C.J., LYNCH, W.T. Lightly Doped Schottky MOSFET. *IEDM*, 1982; pp. 466-469.	☐	☐
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		TSUI, B., CHEN, M. A Novel Process for High-Performance Schottky Barrier PMOS. *J. Electrochem Soc.*, Vol. 136, No. 5, May 1989; pp. 1456-1459.	☐	☐
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		ZHAO, Q.T., KLINKHAMMER, F., DOLLE, M., KAPPIUS, L., MANTL, S. Nanometer Patterning of Epitaxial CoSi2/Si(100) for Ultrashort Channel Schottky Barrier Metal-Oxide-Semiconductor Field Effect Transistors. *Applied Physics Letters*, Vol. 74, No. 3, 18 January 1999; pp. 454-456.	☐	☐
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		SZE, S.M. Physics of Semiconductor Devices, John Wiley & Sons, Second Edition, 1981; pp. 293-294.	☐	☐
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		Web page "provided by Laurie Calvet", "Device Physics of the SBMOSFET", http://www.eng.yale.edu/reedlab/research/semicond.html, date not established; 7 pages.	☐	☐
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		International Technology Roadmap for Semiconductors 1999, US Copyright 1999 by Semiconductor Industry Association, Front End Processes section, page 107.	☐	☐

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		Tu, K.N. Thompson, R.D., Tsaur, B.Y. Low Schottky Barrier of Rare-Earth Silicide on n-Si, *Applied Physics Letters*, vol. 38, No. 8, Apr. 1981; pp. 626-628.	☐	☐
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		Taur, Yuan. The Incredible Shrinking Transistor. *IEEE Spectrum*, Jul. 1999; pp. 25-29.	☐	☐
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